Development of Radiation-hard Electronics for the ATLAS Detector at LHC

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Overview

- Groups at UoC, ANL, FNAL request $100K seed funding to perform R&D towards a proposal to upgrade the ATLAS experiment Tile Calorimeter electronics
- Relies heavily on electronics groups:
  - J-F Genat at UoC Electronics Development Grp
  - Ray Yarema at FNAL Physics electronics group
  - Gary Drake at ANL HEP electronics group

Background

- The UoC Electronic Development group designed much of the on-board electronics for the ATLAS hadron calorimeter.
- The ANL HEP was heavily involved in calorimeter construction, and led the repairs of the LVPS system
- TileCal is a very important component!

Background (2)

- in 6-7 years much of the electronics must be replaced:
  - super-LHC will run at higher luminosity
    - thus higher radiation doses
  - there are no longer replacements for some crucial components
  - many commercial components with much better performance are available
  - LVPS design was not optimal

Why use UoC/FNAL/ANL $?

- Many ATLAS institutions have expressed interest in participating in the upgrade
  - those that initiate R&D will be the major players…seed funding will really pay off
- The lead time is not very long…we need to start now!

R&D Needed

- Achieving radiation hardness for sLHC is a real challenge:
  - if a commercial rad-hard part exists, it usually costs aerospace prices ($5000 for an FPGA!!!)
  - we cannot find some commercially rated rad-hard components
    - thus we need to perform our own tests and, in some cases, design custom chips
- We also need to incorporate modern communications, power, and trigger upgrades
- Payoff to greater community: LHC, spaceborne astrophysics, future HEP

Expertise

- UoC, ANL, and FNAL electronics groups have some unique areas of expertise
  - UoC: EDG designed originals and has tools and infrastructure for digital and analog front-end circuits
  - ANL: HEP electronics group also has excellent board design infrastructure and will focus on power distribution
    - also radiation test facilities
  - FNAL: has unique expertise in ASIC design which we will need for custom-chip solutions
    - FNAL fits in naturally to addressing this problem!
    - also have radiation-tolerance expertise

Approach

- First identify acceptable components
  - will require conducting radiation exposures
    - design PCBs to test functional radiation tolerance
- Design new front-end circuits
  - radiation tolerant design (ie, reduncancy, voting…)
  - increase dynamic range
  - minimise connections, low-voltage levels
- redesign trigger logic
  - rad-hard communications a real challenge here

2-year Plan

- The project needs 1 FTE engineer for 2 years to get the answers we need before we can submit a new design
  - sets the scale of $100K request
  - if we are only funded for 1 year: still very useful…gets us in the game, but will delay the redesign
- year-1: identify commercially available components & design radiation tolerant architectures; build testing boards
- year-2: conduct radiation tests; possibly design ASICs; design communications

The Team:

- University of Chicago
  - Mark Oreglia
    - Kelby Anderson
    - Jean-Francois Genat (EE)
    - Jim Pilcher
    - Fukun Tang (EE)
- Fermilab
  - Marcel Demarteau
    - Ray Yarema (EE)
- Argonne
  - Lawrence Price
    - Gary Drake (EE)
    - Jimmy Proudfoot
    - Bob Stanek